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Patent Application for:

Controlling Electronics Across an RF Barrier Using a Serial Interface Bus

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5 **Controlling Electronics Across an RF Barrier Using a Serial Interface**

6 **Bus**

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9 TECHNICAL FIELD

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11 This invention relates generally to the field of radio frequency (RF) fixture

12 devices, and more specifically to a method of controlling electronics across an

13 RF barrier.

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15 BACKGROUND OF THE INVENTION

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17 RF enclosures may be used in a variety of test and measurement applications

18 when the amount of RF radiation that impacts a device under test (DUT) must

19 be carefully controlled. Specific examples include prototype testing and

20 production testing of cellular telephones, portable computers, pagers, and

21 other small electronic devices. Often RF enclosures are used in automated or

22 semi-automated environments in which machines are used to place the DUT

23 inside the RF enclosure. In these types of test environments, it is desirable to

24 be able to evaluate the functionality and correct operation of the DUT while

25 the DUT is within the RF enclosure. The use of electronics circuitry and

26 software may be used to apply specific test resources to the DUT and

27 measure the responses. In most applications, the electronics circuitry and

28 software is located both internal and external to the RF enclosure. However,

29 placing high speed electronics within the RF enclosure reduces the RF

30 isolation and generates spurious noise, therefore degrading the testing

31 accuracy. The proximity of the electronics to the DUT also influences the

32 measurement accuracy. Thus, in test and measurement situations involving

33 an RF enclosure, there are often two competing design considerations:

1 Including more sophisticated electronic components within an RF enclosure

2 allows more accurate and more comprehensive test procedures to be

3 executed. However from the point of view of RF isolation and noise reduction

4 , fewer electronics components create smaller amounts of spurious RF energy

5 that leads to improved RF measurements. These competing considerations

6 must both be addressed when designing RF test and measurement systems

7 that incorporate RF enclosures.

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9 A further issue when electronics components are used within an RF enclosure

10 is the complexity of the interface between the electronics inside the RF

11 enclosure and the electronics outside the RF enclosure. As the number of

12 communication paths that cross the RF interface increase, so does the

13 amount of RF noise generated by each path. Thus, a secondary design

14 consideration is the method of controlling the electronics path across an RF

15 barrier of an RF enclosure.

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17 There are many different methods of controlling electronics across an RF

18 barrier of an RF enclosure. The RF enclosure may be used to test and

19 prototype electronics devices, such as cell phones, personal digital assistants

20 (PDAs), and other similar electronics. Most methods of controlling electronics

21 across an RF barrier use electrical signals propagating through a filtered

22 connector as the primary transport mechanism. These electrical signals can

23 carry data reads and data writes to and from the electronics within an RF

24 enclosure. Most of these methods may be classified into one of three basic

25 types: direct drive, wide parallel, and command serial.

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27 A direct drive control method consists of providing dedicated electrical

28 resources outside of the RF enclosure that pass through the filtered

29 connector(s) for each element being controlled. An example of this type of

1   control method would be to generate relay coil drive signals outside the RF

2   cavity and pass each of these drive lines through the filtered connectors to

3   relays inside the cavity. This method requires an individual control line that

4   passes through the filtered connector for each resource being controlled. It is

5   desirable to limit the number of control lines passing through the filtered

6   connectors since these filtered connectors are very expensive (approximately

7   $2.00/line) and the effective RF isolation of the structure degrades with the

8   number of signals passing through the filtered connectors. A direct drive

9   scheme is also not very flexible or expandable.

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11   A wide parallel control method consists of a conventional address, data, and

12   control scheme in which all signals must pass through the filtered

13   connectors(s) to register based electronics inside the RF cavity. This method

14   often requires a large number of signals passing through the filtered

15   connectors. A typical implementation might consist of 16 or more lines: 8

16   data, 5 address, and 3 control. Many RF test fixtures such as the TS-50

17   (Yukon) and the Z2030A (Osprey) use this control method.

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19   A command serial control method consists of sending commands across the

20   filtered connector(s) to a microprocessor or other programmable logic device

21   that can interpret these commands into control sequences. This method

22   commonly requires a clock to be running at all times inside the RF enclosed

23   portion for clocking the microprocessor or logic device. This clock creates

24   spurious noise that can interfere with the measurements inside the RF cavity.

25   Command serial control methods are also more complicated and often require

26   some firmware programming.

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28   Other methods of control across an RF barrier exist that do not use an

29   electrical connection. An example of this is an optical link. These methods

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1   tend to be more expensive and require a free running clock that adds to the

2   electrical noise inside the RF cavity.

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4   Thus, there is an unmet need in the art for a simple, cost effective method of

5   controlling electronics across an RF barrier. Such a method should provide

6   an ideal environment for test RF devices, have good RF isolation, encompass

7   a less expensive design with fewer lines and built-in interfaces, have low

8   spurious noise, be simple to implement, and be flexible and extensible to

9   future enhancements.

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12   SUMMARY OF THE INVENTION

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15   The present invention takes advantage of the industry standard serial data

16   control buses capable of serially shifting data in and/or out of electronics

17   being controlled in some pre-determined protocol to provide a serial data

18   control protocol for controlling electronics across an RF barrier. A

19   microprocessor with a built-in serial data control bus (e.g., SPI) exists outside

20   of the RF chamber. An address dependent form of the serial bus passes

21   through one or more RF filtered connectors into the RF cavity. The processor

22   uses the serial data bus to control (data reads and data writes) an arbitrary

23   amount of electronics inside and outside of the RF cavity. This control

24   method requires a minimal number of signals passing through the filtered

25   connectors, preserving the RF isolation of the cavity from the external

26   environment.

27

28   The addressing scheme is designed to specifically isolate electronics outside

29   the RF chamber from the electronics inside the chamber. The serial data bus

1   lines that pass through into the RF cavity are held in a quiescent state unless

2   being used to control electronics inside the RF cavity. This signal isolation

3   technique provides a very low spurious noise environment inside the RF

4   cavity. This is important for sensitive RF measurements, while allowing the

5   processor to control external electronics. This gating functionality may

6   additionally have a temporal aspect that controls when individual signals are

7   gated from entering the RF cavity. This provides the important advantage of

8   being able to selectively control noise levels experienced during the testing

9   process.

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12   BRIEF DESCRIPTION OF THE DRAWINGS

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14   The features of the invention believed to be novel are set forth with

15   particularity in the appended claims. The invention itself however, both as to

16   organization and method of operation, together with objects and advantages

17   thereof, may be best understood by reference to the following detailed

18   description of the invention, which describes certain exemplary embodiments

19   of the invention, taken in conjunction with the accompanying drawings in

20   which:

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22   FIG. 1 is a block diagram of an RF cavity and the associated control

23   elements, according to an embodiment of the present invention.

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25   FIG. 2 is a sample addressing scheme, according to an embodiment of

26   the present invention.

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29   DETAILED DESCRIPTION OF THE INVENTION

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2 While this invention is susceptible of embodiment in many different forms,

3 there is shown in the drawings and will herein be described in detail specific

4 embodiments, with the understanding that the present disclosure is to be

5 considered as an example of the principles of the invention and not intended

6 to limit the invention to the specific embodiments shown and described. In the

7 description below, like reference numerals are used to describe the same,

8 similar or corresponding parts in the several views of the drawings.

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10 A number of industry standard serial data control buses exist for controlling

11 electronics using a limited number of electrical lines. These buses serially

12 shift data in and/or out of electronics being controlled in some pre-determined

13 protocol. These buses commonly require a clock line, data line, and possibly

14 one or more control lines. Such control lines may be used for operations such

15 as chip select and chip reset, depending upon the exact bus implementation.

16 Examples of these protocols include Microwire, I2C, SPI, and JTAG Boundary

17 Scan (IEEE1149.1). Industry standard buses are commonly available on

18 many different types of electronics including microprocessors, Digital-to-

19 Analog Converters (DACs), Analog-to-Digital Converters (ADCs), memories,

20 and register-based control devices.

21

22 The present invention is able to use these serial data control buses to provide

23 a serial data control protocol for controlling electronics across an RF barrier.

24 A microprocessor with a built-in serial data control bus (e.g., SPI) exists

25 outside of the RF chamber. An address dependent form of the serial bus

26 passes through one or more RF filtered connectors into the RF cavity. The

27 processor uses the serial data bus to control (data reads and data writes) an

28 arbitrary amount of electronics inside and outside of the RF cavity. This

29 control method requires a minimal number of signals passing through the

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1   filtered connectors, preserving the RF isolation of the cavity from the external

2   environment.

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4   Referring to block diagram 100 of **Figure 1**, an embodiment of the present

5   invention is shown. Processor 120 is coupled to interface electronics 133 via

6   a serial data control bus cable 125. A non-RF cavity 150 is used to house the

7   processor 120 and the electronics outside the RF chamber 160. An external

8   controller 170, such as a personal computer (PC), uses a number of external

9   interfaces 165, either serial or parallel, e.g. RS232, to control the processor

10   120. Interface electronics 133 is operable to choose one or more of a

11   plethora of input signals. The selected input signals are coupled to filtered

12   connector 130. Filtered connector 130 is coupled to electronics 140 within RF

13   cavity 110 by serial data control bus cable 135, which may be physically

14   realized as one or more cables or printed circuit assemblies. Processor 120

15   is operable to transmit and receive one or more data signals using serial data

16   control bus cable 125 to filtered connector 130. Filtered connector 130

17   isolates these one or more data signals and passes them to electronics 140

18   via serial data control bus cable 135. An addressing scheme is implemented

19   by processor 120 so that only those serial bus lines that are used to control

20   electronics 140 within RF cavity 110 are active. The selection of the one or

21   more serial lines operable to enter RF cavity 110 is controlled by interface

22   electronics 133. The use of a gating functionality to determine which signals

23   are permitted to enter RF cavity 110 may additionally have a temporal aspect

24   in that it may be used to selectively determine when such signals are

25   permitted to enter RF cavity 110. This temporal aspect is an important

26   advantage of the present invention. There may be times during the testing

27   process when eliminating spurious noise is not important but other times,

28   such as during noise sensitive measurements, which it can be critical.

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1 Referring now to **Figure 2**, an example of this addressing scheme is shown

2 according to one embodiment of the present invention. This example uses

3 eight addresses to control electronics internal and external to the RF cavity.

4 Addresses 0,1,2, and 3 are operable to control one or more electronics

5 elements within electronics 140. Addresses 4, 5, 6, and 7 are operable to

6 control one or more elements within electronics outside the RF chamber 160.

7 In this example address line #1 is used to gate all signals that enter RF cavity

8 110. Thus only addresses 0, 1, 2, and 3 are active within the RF cavity. This

9 gating functionality, enabled through setting the value of line #1, allows a

10 processor element to allow only those signals used to control electronics 140

11 enter the RF cavity. Those signals corresponding to addresses 4, 5, 6, and 7

12 are held in a quiescent mode within the RF cavity. Again, the gating

13 functionality may have a temporal characteristic in that interface electronics

14 133 can through the gating control when certain signals are allowed to enter

15 RF cavity 110.

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17 Those of ordinary skill in the art will recognize that the present invention has

18 been described in terms of exemplary embodiments. It should be apparent to

19 one of skill in the art that the number of addresses and the method of gating

20 the addresses may differ from that presented in Figure 2. For example, 32

21 addresses could be used, with 24 applied to components within the cavity and

22 8 applied to components external to the cavity. In a preferred embodiment of

23 the present invention, integrated circuit technology is used to provide the

24 quiescent gating function that allows only certain signals to enter the RF

25 cavity. This gating function may have a selective temporal quality that

26 determines when these certain signals are permitted to enter the RF cavity. It

27 should also be apparent to one of skill in the art that many different types of

28 serial data control buses could be implemented without departing from the

29 spirit and scope of the present invention. Microwire, I2C, SPI, and

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1   IEEE1149.1 are some examples of applicable serial data control buses.

2   According to the preferred embodiment of the present invention, SPI is used

3   as the serial data control bus.

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5   It should also be apparent to one or skill in the art that interface electronics

6   133 is operable to be coupled directly to processor 120 without departing from

7   the spirit and scope of the present invention. Further, electronics component

8   140 may be distributed in several locations within RF enclosure 110. Filtered

9   connector 130 is operable to maintain connections with one or more of these

10   distributed electronics components.

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12   While the invention has been described in conjunction with specific

13   embodiments, it is evident that many alternatives, modifications, permutations

14   and variations will become apparent to those of ordinary skill in the art in light

15   of the foregoing description. Accordingly, it is intended that the present

16   invention embrace all such alternatives, modifications and variations as fall

17   within the scope of the appended claims.

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19   What is claimed is:

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